

REMARKS/ARGUMENTS

The Examiner is thanked for the final Office Action mailed February 4, 2008. The status of the application is as follows:

- Claims 1, 2 and 4-21 are pending;
- Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Rocha et al. (ROCHA, J.G., et al, CMOS X-ray Image Sensor with Pixel Level A/D Conversion. IEEE European Solid-State Circuits Conference, (2003), p. 121-124);
- Claims 1, 2, 4 and 6-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boles et al. (BOLES, Colby D., Colby D., Bernhard E. Boser, Bruce H. Hasagawa, and Joseph A. Heanue, "A Multimode Digital Detector Readout for Solid-State medical Imaging Detectors." IEEE Journal for Solid State Circuits 33, No. 5 (1998)) in view of Rocha;
- Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boles et al. in view of Rocha and Ribner (5,142,286).

The rejections are discussed below.

The Rejection of Claims 1 and 2 under 35 U.S.C. 102(b)

Claims 1 and 2 stand rejected under 35 U.S.C. 102(b) as being anticipated by Rocha et al. This rejection should be withdrawn because Rocha et al. does not teach each and every element as set forth in the subject claims and, therefore, does not anticipate claims 1 and 2.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). MPEP §2131.

Independent **claim 1** is directed towards a detector arrangement with a plurality of detector elements. Each of the plurality of detector elements includes an integrated SD modulator, wherein for each detector element *both the detector element and the corresponding integrated SD modulator reside on a same CMOS semiconductor structure* and the SD modulator has a differential design and a plurality of stages. Rocha et al. does not teach or suggest each and every one of the above claim aspects as set forth in claim 1.

The Office asserts that Rocha et al. teaches the above claim aspects at page 121, column 2, page 122, column 1, and page 123, column 1, and in Figure 3. Applicant respectfully traverses this assertion. Page 121, column 2, discloses an x-ray image sensor having an array of blocks, each block containing a photodiode and its own A/D converter, wherein the A/D converter is 120 μm x 270 μm and is fabricated using a standard CMOS nwell 1.6 μm process. Hence, this section of Rocha et al. teaches that the A/D converter is fabricated using a standard CMOS process. However, this section of Rocha et al. does not teach or suggest that both the photodiode and the A/D converter reside on a same CMOS semiconductor structure. The other referenced sections of Rocha et al. do not contemplate the arrangement of the photodiode or the A/D converter within the x-ray image sensor. More particularly, Figure 3 shows a block diagram illustration for one pixel, page 122, column 1, notes that the A/D converter is a SD converter, and page 123, column 1, discusses a 1-bit A/D converter, or comparator.

In view of the foregoing, this rejection should be withdrawn.

Claim 2 depends from claim 1 and is allowable at least by virtue of its dependency.

The Rejection of Claims 1, 2, 4, and 6-21 under 35 U.S.C. 103(a)

Claims 1, 2, 4, 6-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boles et al. in view of Rocha. This rejection should be withdrawn because the combination of Boles et al. and Rocha does not teach or suggest all the limitations of the subject claims and, therefore, fails to establish a *prima facie* case of obvious with respect to the subject claims.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art.
In re Royka, 490 F.2d 981, (CCPA 1974). MPEP §2143.03.

With respect to **claim 1**, the Office concedes that Boles does not teach or suggest a detector arrangement in which *both the detector element and the corresponding integrated SD modulator reside on a same CMOS semiconductor structure*. In an attempt to make up for this conceded deficiency, the Office references Rocha et al. and states that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Boles with the disclosure of Rocha et al. to teach claim 1. However, as discussed above, the sections of Rocha et al. cited by the Office do not teach or suggest such claim aspects. Rather, they disclose an x-

ray image sensor having an array of blocks, wherein each block contains a photodiode and an A/D converter that is fabricated using a standard CMOS nwell 1.6 μm process. Hence, Rocha et al. does not make up for the conceded deficiency, and this rejection should be withdrawn.

Claims 2, 4 and 6-9 depend from claim 1 and are allowable at least by virtue of their dependencies.

Independent **claim 10** recites aspects similar to those recited in claim 1. As such, the discussion of claims 1 applies *mutatis mutandis* to claim 10 and, therefore, the rejection of claim 10 should be withdrawn.

Claims 11-15 depend from claim 10 and are allowable at least by virtue of their dependencies.

Claim 16, which indirectly depends from claim 10, recites that the decimation filter converts *differential one (1) bit data streams* from the Sigma Delta Analog-to-Digital component into a single seventeen (17) bit data signal. The Office asserts that Boles discloses a decimation filter that converts a 1-bit output stream of a SD A/D converter to a 20-bit signal. However, this section of Boles does not teach or suggest that the 1-bit output stream is a *differential* stream. Therefore, this rejection should be withdrawn.

Independent **claim 17** is directed towards a method that includes, *inter alia*, detecting radiation with a first component, producing a first signal indicative of the detected radiation, generating a second signal, based on the first signal, with a second component, wherein *the first and second components reside on a same integrated chip (IC)*. The Office asserts that Boles teaches all of these claim aspects. More particularly, the Office asserts that Table 1 and the Introduction of Boles teach a photodetector and a SD A/D converter that reside on a same chip. In contrast, the referenced sections of Boles expressly states interfacing an IC, which includes a SD A/D converter, to a photodetector array that detects both SPECT and CT data. Thus, Boles expressly states that the photodetector and the SD A/D converter do not reside on the same IC. In view of the foregoing, it is readily apparent that Boles does not teach or suggest all of the claim aspects of claim 17. Accordingly, this rejection should be withdrawn.

Claims 18-20 depend from claim 17 and are allowable at least by virtue of their dependencies.

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Claim 21, which depends from claim 17, recites the method further includes *continuously integrating* the first signal and generating the second signal based thereon. The Office asserts Boles teaches this claim aspect in Section III, B, 2. However, the subject section of Boles is silent regarding such a teaching. Instead, this section of Boles provides various integrator design factors. Thus, the rejection of claim 17 should be withdrawn.

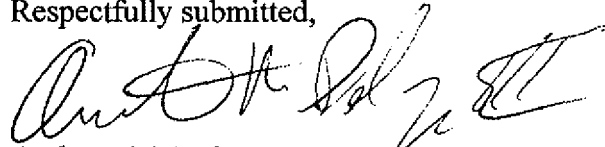
The Rejection of Claim 5 under 35 U.S.C. 103(a)

Claim 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boles et al. in view of Rocha and Ribner. This rejection should be withdrawn as claim 5 is allowable at least by virtue of its dependency to an allowable base claim.

Conclusion

In view of the foregoing, it is submitted that the claims distinguish patentably and non-obviously over the prior art of record. An early indication of allowability is earnestly solicited.

Respectfully submitted,



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